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# Inversion Channel MOSFETs in 3C-SiC on Silicon

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## Abstract

As a substrate material, single crystal SiC wafers are commercially available in diameters up to 75 mm, whereas silicon wafers are available in diameters of 200 – 300 mm. SiC wafers remain quite expensive compared to silicon, and contain troublesome densities of micropipes that limit the yield of large devices. In the past, several groups have attempted to circumvent these problems by fabricating devices in 3C-SiC films grown epitaxially on silicon substrates, with limited success. However, in this paper we report new results demonstrating high quality inversion channel MOSFETs in 3C-SiC films on silicon.

The inversion channel mobility of SiC MOSFETs has been limited to  $< 50 \text{ cm}^2/\text{Vs}$  in the 4H polytype and  $< 100 \text{ cm}^2/\text{Vs}$  in the 6H polytype by a high density of interface states in the upper half of the bandgap. Because of its narrower bandgap, the 3C polytype of SiC is expected to have lower interface state density, leading to higher channel mobilities.

We fabricated lateral n-channel MOSFETs in 6  $\mu\text{m}$  p-type epilayers of 3C-SiC grown on 2° off-axis Si(001) substrates. The epilayers were subsequently polished to improve surface smoothness, leaving a 3  $\mu\text{m}$  layer. Sacrificial oxidation was then performed to remove damage caused by polishing. Source and drains were formed by implanting phosphorus and activating at 1250 °C for 30 minutes in argon. The gate oxide was formed by wet oxidation at 1150 °C for 30 minutes, followed by re-oxidation in wet O<sub>2</sub> at 950 °C for two hours. A polysilicon gate was deposited by LPCVD and doped by spin-on dopant. Ohmic contacts are unannealed nickel. The resulting MOSFETs show excellent transistor behavior, with good current saturation, a threshold voltage of 1.6 V, and a peak channel mobility of 170  $\text{cm}^2/\text{Vs}$ .

## I. Introduction

Because of its wide band gap (2.2eV-3.2eV depending on polytype) and excellent thermal conductivity, silicon carbide (SiC) is an ideal semiconductor material for high power, high voltage and high temperature applications. While many high performance power devices have been demonstrated on 4H- and 6H-SiC wafers [1-3], far fewer devices on 3C-SiC have been demonstrated. There exists no substrates of 3C polytype, and 3C epilayers are grown heteroepitaxially on large area silicon substrates by chemical vapor deposition (CVD) [4]. Earlier attempts in 1980's to fabricate metal-oxide-semiconductor field-effect transistors (MOSFET) in 3C-SiC showed large drain leakage current [5] or poor current saturation [6].

These poor results were due to the high defect density in 3C-SiC epilayers and poorly developed process techniques for 3C-SiC devices.

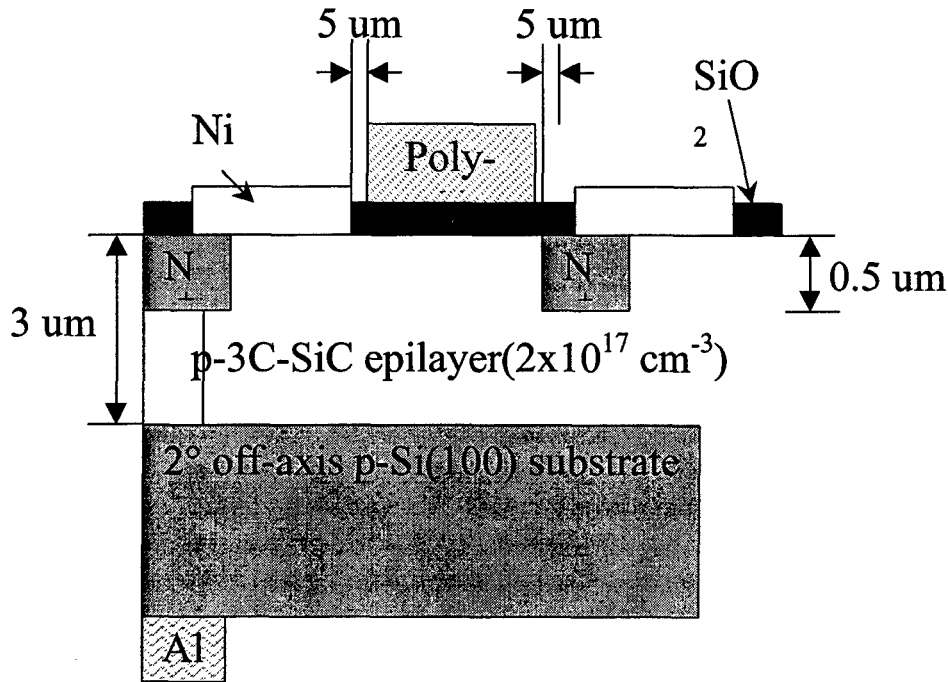
The improvement of 3C-SiC epitaxial growth and the availability of more mature SiC processing technology have lead to a renewed interest in 3C-SiC materials and devices. The inversion channel mobility of SiC MOSFETs has been limited to  $< 50 \text{ cm}^2/\text{Vs}$  in the 4H polytype and  $< 100 \text{ cm}^2/\text{Vs}$  in the 6H polytype by a high density of interface states in the upper half of the bandgap. In contrast, 3C-SiC MOSFET's have demonstrated an effective channel mobility about  $100 \text{ cm}^2/\text{Vs}$  [6]. The potential for integrating SiC with Si technology has also become feasible with the improvements made in SiC processing. In this paper, we report inversion-type n-channel 3C-SiC MOSFET's fabricated on Si(001) substrates which show excellent transistor behavior and a channel mobility of  $170 \text{ cm}^2/\text{Vs}$ . Subthreshold characteristics and gate oxide integrity are also evaluated.

## II. Device fabrication

A 6- $\mu\text{m}$ -thick, p-type 3C-SiC ( $2 \times 10^{17} \text{ cm}^{-3}$ ) epilayer was grown on a  $2^\circ$  off-axis p-type Si(001) substrate by CVD, with silane and propane as precursors. The epilayer was subsequently polished by a chemical mechanic polishing (CMP) process to improve surface smoothness, leaving a 3  $\mu\text{m}$  layer. Sacrificial oxidation was performed to remove lattice damage caused by polishing. A carefully-designed phosphorus implantation scheme, including four implantations, with energies and doses of  $360 \text{ keV}/1.5 \times 10^{15} \text{ cm}^{-2}$ ,  $220 \text{ keV}/1.1 \times 10^{15} \text{ cm}^{-2}$ ,  $100 \text{ keV}/8 \times 10^{14} \text{ cm}^{-2}$  and  $30 \text{ keV}/6 \times 10^{14} \text{ cm}^{-2}$ , respectively, was employed to form a uniform doping profile in the source and drain regions of the MOSFET. The resulting source/drain junction depth was about 500 nm. The implantation mask was a Ti(10 nm)/Au(80 nm) metal bilayer. Following implantation, the sample was annealed at  $1250^\circ\text{C}$  for 30 minutes in argon to activate the implanted dopants. An RCA cleaning procedure was performed immediately before the sample was loaded into a pyrogenic oxidation system. An oxidation procedure optimized for 4H-SiC was used, which consisted of wet oxidation at  $1150^\circ\text{C}$  for 2.5 hours, argon annealing at  $1150^\circ\text{C}$  for 30 minutes, and reoxidation at  $950^\circ\text{C}$  for 2 hours. The oxidation rate of 3C-SiC is about 2-3 times higher than that of 4H-SiC and, therefore, the oxidation time was reduced to 40 minutes to produce an 80-nm-thick gate oxide. A poly-silicon gate (400 nm thick) was deposited by LPCVD and was subsequently doped by spin-on phosphorus dopant. The gate was defined using wet etching ( $\text{HNO}_3:\text{HF}:\text{H}_2\text{O}=55:3:30$ ). Finally, contact windows were opened in the source and drain regions by wet etching the oxide, and a 200 nm-thick nickel layer was evaporated to form ohmic contacts. Aluminum was deposited on the backside of the sample to form an ohmic contact to the p-type silicon substrate. Due to processing constraints, alloying of ohmic contacts was not performed yet.

Figure 1 shows a schematic cross-section of the 3C-SiC MOSFET device. Devices with a gate width of  $110 \mu\text{m}$  and various gate lengths of 3, 5, 10, 20, 50, 80, 110 and  $140 \mu\text{m}$  were fabricated. All devices were a planar structure with a strip gate layout. Transmission line

method (TLM) test structures were also fabricated to monitor contact resistance and sheet resistance of the implanted regions. Circular MOS capacitors with a diameter of  $450\text{ }\mu\text{m}$  were designed in front-to-front configuration for MOS C-V measurements.



**Figure 1:** The schematic cross section of a 3C-SiC MOSFET

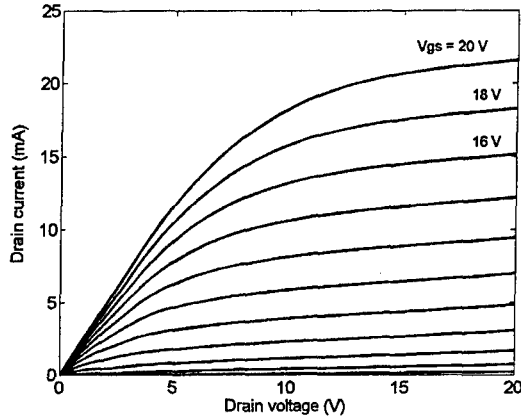
### III. Results and discussion

As-deposited Ni contacts on the implanted SiC layer exhibit an ohmic characteristic with contact resistivity of  $4.2 \times 10^{-3}\text{ ohm-cm}^2$  measured from TLM structures. The sheet resistance of the implanted regions is about  $70\text{ }\Omega$  per square, which is nearly equivalent to previously reported data [7].

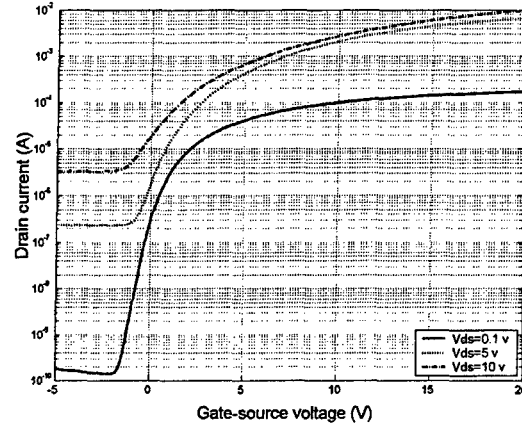
The drain characteristics of MOSFETs were measured by a HP4156 semiconductor parameter analyzer. Figure 2 shows the drain current ( $I_D$ ) versus drain voltage ( $V_{ds}$ ) curves, with gate voltage ( $V_{gs}$ ) from 0 to 20 V in steps of 2 V, for a device with a gate length of 3  $\mu\text{m}$ . Current saturation is observed for positive gate biases while the device can be properly turned off at zero gate bias.

The subthreshold characteristics were examined by measuring drain current ( $I_D$ ) versus gate voltage ( $V_{gs}$ ) at a fixed drain voltage ( $V_{ds}$ ). Figure 3 shows  $I_{ds}$  versus  $V_{gs}$  curves at three different  $V_{ds}$  bias of 0.1, 5, 10 V, respectively, for a device with a gate length of 5  $\mu\text{m}$ . At

$V_{ds} = 0.1$  V, the device has a small leakage current and the subthreshold slope is about 391 mV/decade. At higher  $V_{ds}$ , the leakage current is increased significantly. Defects in 3C-SiC epilayer are responsible for the leakage current and further improvement in crystal quality are needed to alleviate this problem. From the linear plot of  $I_D$  versus  $V_{gs}$ , the threshold voltage of this device is 1.6 V.



**Figure 2:** Drain characteristics of a 3C-SiC MOSFET with a gate length of 3  $\mu\text{m}$  ( $V_{GS}$  varied from 0 to 20 V in steps of 2V)



**Figure 3:** Subthreshold characteristics of a 3C-SiC MOSFET with a gate length of 5  $\mu\text{m}$  ( $V_{DS}$  values of 0.1 V, 5 V, and 10 V).

The channel mobility was estimated by differentiating  $I_D$  with regard to  $V_{gs}$  in the linear region ( $V_{ds} = 0.1$  V) using equation (1).

$$\mu = \frac{L}{WC_{ox}V_{ds}} \frac{\partial I_d}{\partial V_{gs}} \quad (1)$$

where  $L$  and  $W$  are gate length and width, respectively,  $C_{ox}$  is the gate oxide capacitance for unit area. Figure 4 shows the dependence of channel mobility on gate voltage for a device with a gate length of 140  $\mu\text{m}$ . A peak mobility of 170  $\text{cm}^2/\text{Vs}$  was observed at a gate voltage of about 12 V, while the channel mobility gradually decreased at a higher gate voltage.

MOS capacitors were measured using a HP4284 LCR meter. Figure 5 shows a capacitance-voltage curve of a 3C-SiC MOS structure at 10 KHz taken in the dark. It is interesting to note that inversion was observed even without illumination and the C-V curve exhibited a peculiar “hook and ledge” characteristics similar to previously reported 6H-SiC results [8]. To understand this strange C-V curve, both fixed charges and interface traps should be taken into account together with the particular configuration of the MOS capacitor structures. The measured circular MOS capacitor is surrounded by a large area capacitor. From the C-V curve in figure 5, we can see a large negative shift in the flat band voltage (close to -20 V). This suggests a large number of positive fixed charges in the oxide.

Because of these fixed charges, the 3C-SiC surface underneath the large area capacitor could be inverted into n-type, serving as an electron supply for the small area capacitor. When the gate bias on the measured capacitor was swept from -20 V (point A) to 0 V (point B), this MOS capacitor was pushed into deep depletion because electrons supplied from large area MOS capacitor were trapped by interface traps located at the gap between the two capacitors. During this process, the interface traps of the small capacitor were empty. Once the interface traps between the gap were completely filled, electrons were able to begin filling the interface traps underneath the small capacitor and bring the MOS capacitor into inversion (point D). Inversion under the small capacitor always occurs at zero volt, because this is the point where the voltage polarity between the small and large capacitors reverses. When the gate bias was swept back from 10V to -20V, the MOS capacitor went from inversion into accumulation. However, the interface traps of the MOS capacitor were filled during this reverse sweep, which caused a parallel shift of C-V curves with respect to the forward sweep curve at the region from 0 V to -5 V. The voltage shift  $\Delta V_g$  between forward and reverse C-V curves can be used to estimate the interface trap density by equation (2)

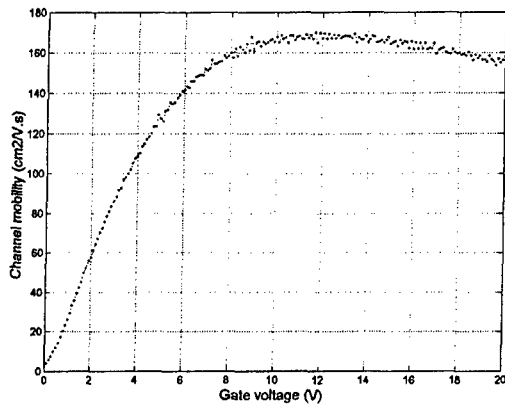
$$N_{IT} = \frac{C_{ox}}{q} \times \Delta V_g \quad (2)$$

Where  $N_{IT}$  is the total interface trap density across the bandgap and  $C_{ox}$  is the oxide capacitance for unit area. According to this calculation, the total interface trap density across 3C-SiC bandgap is about  $1.2 \times 10^{12} \text{ cm}^{-2}$ .

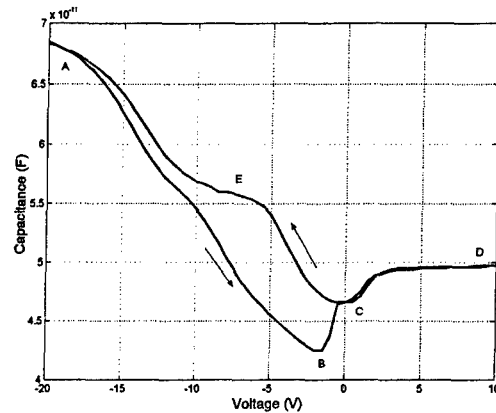
Gate oxide leakage current and breakdown field were also characterized by MOS structures and a typical current-voltage curve is shown in Figure 6. A very low leakage current is observed at electric fields below 3 MV/cm, and breakdown occurs at an electric field of 3.5 MV/cm. This breakdown field is lower than that of the 4H or 6H-SiC oxide (~10 MV/cm) probably due to higher defect density in 3C-SiC. However, this value is higher than the previously reported value of 2.5 MV/cm [9].

#### IV. Conclusions

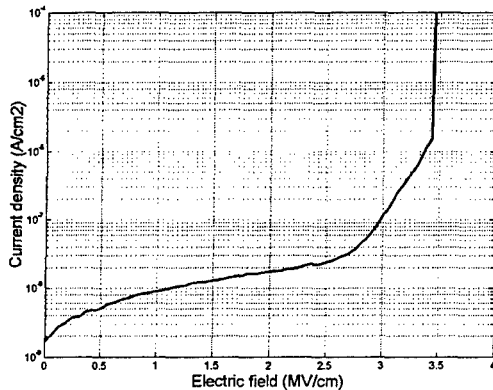
Inversion-mode, n-channel 3C-SiC MOSFETs have been fabricated on 3C-SiC epilayer on silicon substrate. These devices exhibit excellent transistor characteristics and a channel mobility of  $170 \text{ cm}^2/\text{Vs}$ . Capacitance-voltage characteristics of 3C-SiC MOS structures were measured and the interface trap density was estimated to be  $1.2 \times 10^{12} \text{ cm}^{-2}$ . The gate oxide breakdown field is 3.5 MV/cm.



**Figure 4:** Dependence of channel mobility on gate voltage for a device with a gate length of 140  $\mu\text{m}$



**Figure 5:** Capacitance-Voltage curve of a p-3C-SiC MOS capacitor with a diameter of 450  $\mu\text{m}$



**Figure 6:** The leakage current and breakdown field of the gate oxide

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